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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,778	07/31/2003	Fong Shi	60000500.1012	7891

7590 04/06/2005

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,778	SHI, FONG	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17, 27-29, 31-32, 34* is/are rejected.

7)☒ Claim(s) *18,30 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The allowability of claim 5 is withdrawn because the scope of amended claim 5 is changed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 7-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al (US. 6,462,405) in view of Heckaman et al (US. 5,023,624).

Regarding claims 1-4, 12 and 14, Lai (Fig. 2) discloses a near-hermetic semiconductor device comprising: a substrate 40; an integrated circuit 41 disposed on the substrate 40; a lid or sealant 43 disposed on the integrated circuit 41; and a backside interconnect which includes plated-through vias formed in the substrate 40 (not shown, see column 4, lines 14-20), disposed on the integrated circuit 41, connecting the substrate 40 to the sealant-coated integrated circuit 41, and tied to terminal on the substrate (terminal corresponding to conductive traces formed on the substrate (not shown), see column 4, lines 14-20); and a conformal coating 4 disposed on the sealant 43.

Lai does not disclose that the integrated circuit 41 is MMIC.

However, Heckaman (Fig. 1) teaches a hermetic device comprising an integrated circuit of MMIC or Phased Array Antenna (PAA) disposed on the substrate 20 (column

8, lines 40-50). Accordingly, it would have been obvious to form the integrated circuit of Lai as MMIC or PAA because it is an intended use depending upon the electronic application which is desired for the package device, as taught by Heckaman (column 8, lines 40-50).

Regarding claim 7, Heckaman further teaches the forming of a high performance support substrate (e.g., GaAs) for high frequency applications (column 1, lines 19-21).

Regarding claim 10, Lai's (Fig. 2) further discloses the solder attachment 42 formed along a periphery of the integrated circuit 41 to seal the integrated circuit 41 to the substrate 46.

Regarding claim 11, it would have been obvious to form the solder attachment 42 made of AuSn because AuSn is a well-known solder material which has a low melting point.

Regarding claim 8, Lai's (Fig. 2) further discloses that the device is substantially free of bond wires. It would have been obvious to substitute the solder balls 42 with the solder bumps because they are both well-known in the art for providing the electrical contacts between the chip and the substrate in the flip-chip technology.

Regarding claim 9, it would have been obvious to connect the plurality of rest vias of substrate 40 to the ground plane of the substrate in order to provide the external ground terminals for the device package.

4. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo et al (US. 6,525,420) in view of Chun et al (US. 6,710,542).

Zuo (Fig. 4) discloses a near-hermetic device comprising: a substrate 7; an

electronic package 9 disposed on the substrate 7; a backside interconnect formed in the substrate 7, which connects the substrate 7 to the electronic package 9 (not shown, see column 4, lines 20-24); and an attached solder 13 to seal the electronic package 9 to the substrate 7.

Zuo does not disclose an interlayer dielectric disposed between a sealant and the electronic package.

However, Chun (Fig. 2) teaches a near-hermetic device comprising a sealant 22 disposed on the electronic package, and an interlayer dielectric 21 disposed between the sealant 22 and the electronic package. Accordingly, it would have been obvious to modify the semiconductor package of Zuo by forming the sealant and the interlayer dielectric with the structures as set forth above because as taught by Chun, such sealant and interlayer dielectric structures would provide a sealing layer which prevents the moisture and oxygen from reaching the electronic package (column 4, lines 11-17).

5. Claims 6, 27-29, 31-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo et al (US. 6,525,420) in view of Chun et al (US. 6,710,542) and Heckaman et al (US. 5,023,624).

Regarding claims 6 and 27-29, as discussed in details above, the combination of Zuo and Chun substantially reads on the invention as claimed, including the sealant 22 disposed over benzocyclobutene 21 (column 4, lines 9-21) for providing a sealing layer which prevents the moisture and oxygen from reaching the integrated circuit, as taught by Chun (see Fig. 2 and column 4, lines 11-17).

Neither Zuo nor Chun discloses that the integrated circuit is MMIC.

However, Heckaman (Fig. 1) teaches a hermetic device comprising an integrated circuit of MMIC or Phased Array Antenna (PAA) disposed on the substrate 20 (column 8, lines 40-50). Accordingly, it would have been obvious to form the integrated circuit of Zuo as MMIC or PAA because it is an intended use depending upon the electronic application which is desired for the package device, as taught by Heckaman (column 8, lines 40-50).

Regarding claim 31, Heckaman further teaches the forming of a high performance support substrate (e.g., GaAs) for high frequency applications (column 1, lines 19-21).

Regarding claim 32, Zuo (Fig. 4) further discloses the solder attachment 13 formed along a periphery of the integrated circuit 9 to seal the integrated circuit 9 to the substrate 7.

Regarding claim 34, Zuo (Fig. 4) also discloses a cover 20 disposed on the integrated circuit 9.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al (US. 6,462,405) in view of Okuaki (US. 4,814,943).

Lai (Fig. 2) discloses a hermetic semiconductor device, comprising: a substrate 40; an integrated circuit 41 disposed on the substrate 40; a sealant 43 disposed on the integrated circuit; a backside interconnect formed in the substrate 40 or 30 (not shown, see column 4, lines 14-20), which connects the substrate 40 to the sealant-coated integrated circuit; and a conformal coating 4 disposed on the sealant. It is noted that forming the integrated circuit 41 as a Monolithic Microwave Integrated Circuit (MMIC)

would have been obvious because it is an intended use depending upon the electronic application which is desired for the package device.

Lai does not disclose a cover disposed on the package device without directly contacting the coating.

However, Okuaki (Fig. 8) teaches the forming of a cover 28 on the package device without directly contacting the coating 59. Accordingly, it would have been obvious to modify the package device of Lai by forming a cover with the structure as set forth above because as taught by Okuaki, such cover would provide a hermetically sealing for the package device (see abstract).

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al and Heckaman et al as applied to claim 12 above, and further in view of Okuaki (US. 4,814,943).

Neither Lai nor Heckaman discloses a cover disposed over the conformal-coated integrated circuit in a non-contacting manner.

However, Okuaki (Fig. 8) teaches the forming of a cover 28 on the package device without directly contacting the coating 59. Accordingly, it would have been obvious to modify the package device of Lai by forming a cover with the structure as set forth above because as taught by Okuaki, such cover would provide a hermetically sealing for the package device (see abstract).

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ross (US. 5,572,070) in view of Lai et al (US. 6,462,405).

Ross (Fig. 3) discloses a near-hermetic high frequency semiconductor device

(column 1, lines 39-42), comprising: a substrate 14; a high frequency integrated circuit 13 disposed on the substrate 14; and a sealant 20 disposed on the integrated circuit 13 comprising a layer containing particles of alumina or silicon carbide (column 6, lines 1-4 and lines 61-65).

Ross does not specifically disclose a backside interconnect extending between opposite surfaces of the substrate 14 and electrically connecting the substrate 14 to the integrated circuit 13.

However, Lai (Fig. 1) teaches the forming of a backside interconnect extending between opposite surfaces of the substrate 30 and connecting to terminals or conductive traces on the substrate 30 (not shown, see column 4, lines 14-20). Accordingly, it would have been obvious to form a backside interconnect extending between opposite surfaces of the substrate 14 and connecting to conductive traces or terminals of Ross, because as taught by Lai, such backside interconnect structure is well known and commonly used for electrical connecting the substrate to the integrated circuit chip (column 4, lines 20-25). It also would have been obvious to form the integrated circuit 13 of Ross as MMIC because the integrated circuit 13 of Ross suitable for operating at a high-wattage and a high operation frequency (column 1, lines 1-4 and lines 39-42).

Allowable Subject Matter

9. Claims 18, 30 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- In dependent claim 18, the prior art fails to disclose the combination of the semiconductor device structure as recited, including the device being substantially free of solder balls and bond pads and the coating being a low dielectric having a dielectric constant suitable for operating at a frequency of between 2 GHz and 10 GHz.
- In dependent claim 30, the prior art fails to disclose the combination of the semiconductor device structure as recited, including the sealant comprising a layer of silicon carbide.
- In dependent claim 33, the prior art fails to disclose the combination of the semiconductor device structure as recited, including a conformal coating disposed on the sealant.

Response to Arguments

10. Applicant's arguments filed 1/11/05 have been fully considered but they are not persuasive.

Issue No. 1: claims 1-4, 7-12 and 14 are rejected under 35 U.S.C. 103(a) over Lai in view of Heckaman.

Applicant argues that Lai (Fig. 2) does not disclose a backside interconnect structure as claimed because Lai describes vias extending between opposite surfaces of the substrate.

It appears Applicant argues that the backside interconnect must be the vias extending between opposite surfaces of the chip (MMIC). However, the feature of having the backside interconnect comprising the vias extending between opposite

surfaces of the chip does not seem to be required by the claim language. Therefore, Lai does disclose the backside interconnect as claimed because the backside interconnect of Lai is defined as the vias extending between opposite surfaces of the substrate 40 (not shown, see column 4, lines 14-20). These vias are disposed on the chip 41, tie to terminals or conductive traces on the substrate 40 (column 4, lines 14-20), and electrically connect the substrate 40 to the chip 41 (column 4, lines 20-25).

Issue No. 2: claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo in view of Chun.

Applicants argues that Zuo (Fig. 4) does not disclose a backside interconnect structure as claimed because Zuo describes vias extending between opposite surfaces of the substrate.

It appears Applicant argues that the backside interconnect must be the vias extending between opposite surfaces of the chip (MMIC). However, the feature of having the backside interconnect comprising the vias extending between opposite surfaces of the chip does not seem to be required by the claim language. Therefore, Zuo does disclose the backside interconnect as claimed because the backside interconnect of Zuo is defined as the vias or wiring layers extending between opposite surfaces of the substrate 7 (not shown, see column 4, lines 20-23). These vias are disposed on the chip 9, tie to terminals or conductive traces on the substrate 7, and electrically connect the substrate 7 to the chip 9 (column 4, lines 20-23).

Applicant further argues that Zuo does not disclose an interlayer dielectric disposed between a sealant and the electronic package as claimed.

It should be noted that the rejection of claims 15-16 is not based on anticipation, but rather, is based on obviousness. The examiner relies on the combined teachings of Zuo and Chun. Zuo is not relied on for teaching an interlayer dielectric disposed between a sealant and the electronic package as asserted by Applicant, but rather, Chun is relied on for showing that it was known to form an interlayer dielectric disposed between a sealant and the electronic package for preventing the moisture and oxygen from reaching the electronic package (column 4, lines 11-17). The examiner thus regards Applicant's assertions as constituting evidence that Applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

Issue No. 3: claims 6, 27-29, 31, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo in view of Chun and Heckaman.

Applicant argues that Zuo does not disclose a sealant disposed over BCB interlayer dielectric, Chun does not disclose a backside interconnect connecting the substrate to the chip, and Heckaman does not disclose a sealant disposed on the chip or a backside interconnect connecting the substrate to the chip.

It should be noted that the rejection of claims above is not based on anticipation, but rather, is based on obviousness. The examiner relies on the combined teachings of Zuo, Chun and Heckaman. Chun is not relied on for teaching a backside interconnecting the substrate to the chip as asserted by Applicant, but rather, Zuo is relied on for showing that it was known to form a backside interconnect connecting the

substrate to the chip (the discussions with respect to Zuo above in conjunction with **Issue No. 2** are herein incorporated by reference).

Similarly, Zuo or Heckaman is not relied on for teaching a sealant disposed over BCB interlayer dielectric, but rather, Chun is relied on for showing that it was known to form a sealant disposed over BCB interlayer dielectric for preventing the moisture and oxygen from reaching the electronic package (column 4, lines 11-17), and Heckaman is relied on for showing that it was known to form the integrated circuit as MMIC or PAA because it is an intended use depending upon the electronic application which is desired for the package device (column 8, lines 40-50). The examiner thus regards Applicant's assertions as constituting evidence that Applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

Issue No. 4: claims 17 is rejected under 35 U.S.C. 103(a) over Lai in view of Okuaki, and claim 13 is rejected under 35 U.S.C. 103(a) over Lai and Heckaman in view of Okuaki.

Applicant again argues that it would not obvious to combine the references as suggested because Lai (Fig. 2) does not disclose a backside interconnect structure as claimed.

This argument is not persuasive because Lai does disclose a backside interconnect structure as claimed. The discussions with respect to Lai above in conjunction with **Issue No. 1** are herein incorporated by reference.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
April 1, 2005

PHAT X. CAO
PRIMARY EXAMINER